Reducing Phase Noise by Proper Sizing of MOSFETs in LC Tuned VCOs

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Abstract *— This work identifies the relationships between the sizes of the oscillator's core MOSFETs and the phase noise in the $1/f^2$ region. Three packaged 1 GHz VCOs with the same LC tank circuit, but different gate lengths were designed and fabricated in a standard digital 0.6 μm CMOS technology. The minimum gate length (L_{min}) of the core MOSFETs does not result in the minimum phase noise. Instead, the minimum phase noise occurs when the gate length is L_{opt}, and $L_{opt} = \eta \cdot L_{min}$ where η is a parameter that depends upon fabrication process and bias current. From measured results, the phase noise can be further decreased by 2 dBc/Hz at 600 kHz offset from 1 GHz center frequency by using the optimal sizes of the core MOSFETs.*

I. Introduction

An integrated voltage-controlled oscillator is an essential building block in modern communication systems, and low phase noise is a critical parameter for good system performance. Many works report techniques for designing a low phase noise VCO for GHz applications [1]-[3]. However, all of these works achieved the minimum phase noise with a certain frequency offset from the carrier by using the minimum gate length permitted for the MOSFETs in their designs. The reason for using minimum gate length stems from minimizing the parasitic capacitances so that the tuning range can be kept as large as possible. This work shows that the phase noise in the $1/f^2$ region can be further decreased by about 2 dBc/Hz without introducing severe degradation of the tuning range by sizing the core MOSFETs. In section II, a worse case modeling method of the on-chip spiral inductor for the design phase is developed, and a practical LC tank circuit model with associated parasitics for the 1 GHz VCOs is presented. In section III, the noise sources associated with the LC tank circuit and core MOSFETs are identified. Based on the linear and time-varying (LTV) phase noise model [4], the optimum channel length, L_{opt}, for minimum phase noise in the $1/f^2$ is derived. In Section IV, three 1 GHz VCOs with identical LC tank circuits, but different MOSFET sizes are designed, and the measurement results are presented. Finally, Section V gives the conclusions and recommendations for this work.

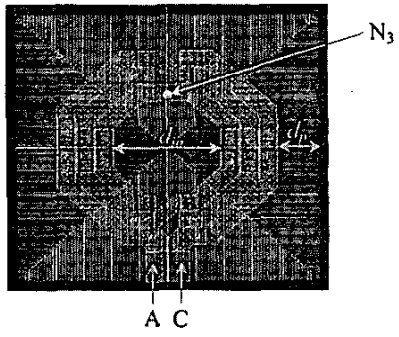

Fig. 1. A symmetrical, octagonal 4 nH inductor with a poly patterned-ground-shield (PGS). Node N_3 is treated as a virtual ground from the differential signal point of view.

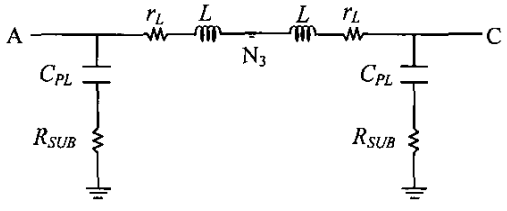

Fig. 2. The lumped-element circuit model for the inductor shown in Fig. 1.

II. A Worse Case Modeling Method Of The On-Chip Spiral Inductor

Many methods for designing an on-chip inductor have been reported [5]-[7]. However, these model parameters are obtained after characterizing the test structures. Therefore, it is desired to develop a modeling technique of the on-chip spiral inductor for the design phase. Figure 1 shows a symmetrical, octagonal 4 nH inductor with a poly patterned-ground-shield (PGS) implemented in a 0.6 μm, 3-metal-layer, 5 V, N-well, and p-epi standard digital CMOS process. Three metal layers are shunted together to reduce the series resistance of the inductor. The width of the metal trace is 40.05 μm, and the spacing between adjacent traces is 1.95 μm. The diameter of the most inner

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turn, d_{in}, is 231.9 μm. The distance between the outmost metal trace and the ground contacts of the PGS, d_p, is 88.8 μm. Figure 2 shows the lumped-element circuit model for this inductor model, which consists of r_L, L, C_{PL}, and R_{SUB}, where r_L is the parasitic series resistance of the inductor, L. C_{PL} models the parasitic capacitance from the metal trace of the inductor to the PGS, and R_{SUB} models the substrate resistance. The methods for modeling parameters (r_L, L, and C_{PL}) have been reported in [8]. With these three parameters (r_L =1.11 Ω, L =1.97 nH, and C_{PL} =4.63 pF), the inductor Q, Q_L , can be calculated by sweeping both frequency and R_{SUB}, and this results in a three-dimensional mesh plot as shown in Figure 3. Since the frequency of interest is 1 GHz, a slicing of this mesh plot at 1 GHz results in a concave upward curve as shown in Figure 4. The inductor Q reaches its minimum, 2.9, when the substrate resistance is 24.45 Ω.

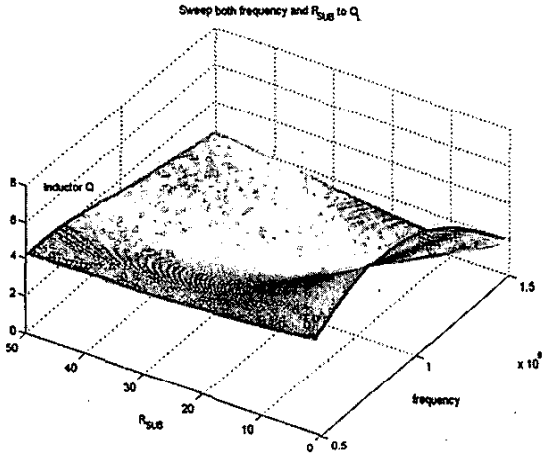


Fig. 3. A mesh plot of inductor Q versus the frequency and R_{SUB}.

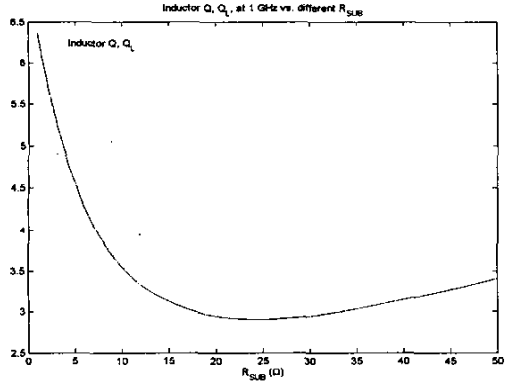


Fig. 4. A slicing of Fig. 3 at the frequency of 1 GHz.

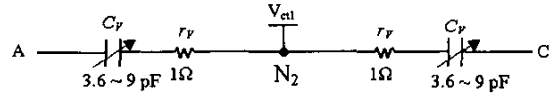


Fig. 5. The lumped-element circuit model for the varactor. Node N_2 is connected to a dc supply and is treated as an AC ground.

Figure 5 shows the lumped-element circuit model for the varactor, which is implemented by a two-terminal type PMOS. The parasitic capacitance associated with the core MOSFETs and buffers is estimated to be around 6 pF [8]. Parameter r_V (estimated as 1 Ω) represents the series resistance of the varactor, C_V. The capacitance of the varactor is designed so that the target center frequency of the oscillator is 1 GHz.

III. Noise Sources Analysis

Figure 6 shows a complementary type VCO with noise sources associated with the passive LC tank circuits and core MOSFETs. The noise current spectrum density generated in the LC tank circuit can be expressed as:

$$\frac{\overline{i_{n,\tan k}^2}}{\Delta f} = 4kT\left[\frac{\omega^2 C_V^2 r_V}{1+\omega^2 C_V^2 r_V^2} + \frac{r_L}{r_L^2+\omega^2 L^2} + \frac{\omega^2 C_{PL}^2 R_{SUB}}{1+\omega^2 C_V^2 r_V^2}\right] \quad (1)$$

where k represents Boltzmann's constant, T is absolute temperature, and Δf is the bandwidth over which the noise is measured.

Hershenson et. al. [9] provide the relationships for predicting channel and gate noise currents in MOSFETs. In Figure 6, the thermal noise current spectrum density of the channel is modeled by

$$\frac{\overline{i_{Md}^2}}{\Delta f} = \frac{4kT\gamma I_{dc}}{E_{sat} L} \equiv \frac{\alpha_1}{L} \text{ and } \alpha_1 = \frac{4kT\gamma I_{dc}}{E_{sat}} \quad (2)$$

where $\gamma \approx 2$ for short channel transistors, I_{dc} is the dc drain current of the MOSFET (or $0.5 \cdot I_{BIAS}$), E_{sat} is the electric field at which the carrier velocity reaches its saturation velocity [12], and L represents the gate length of the MOSFET. The transistor's gate noise current spectrum density is modeled by

$$\frac{\overline{i_{Mg}^2}}{\Delta f} = \left(\frac{4kT\delta\omega^2 C_{gs}^2 E_{sat}}{5 I_{dc}}\right) L \quad (3)$$

where $\delta \approx 2\gamma$, C_{gs} is the gate-to-source capacitance, and ω is the oscillation frequency.

Based on the linear and time-varying phase noise model presented in [4], the single sideband phase noise, Φ_{noise}, in the $1/f^2$ region at an offset frequency, f_{off}, is given by

$$\Phi_{noise}(f_{off}) = \left[\frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^2 q_{\max}^2}\right]\cdot\left[\sum\frac{\overline{i_n^2}}{\Delta f}\right] \quad (4)$$

where Γ_{rms} is the root mean square value of the impulse sensitivity function of the oscillation waveform. For a symmetrical sine wave, Γ_{rms} is 0.5. The maximum charge displacement across the total effective capacitor of the LC tank circuit is denoted as $q_{\max}$. For a given offset frequency, f_{off} can be treated as a constant, and the phase noise is reduced by minimizing the summation of the total noise current spectrum density. Moreover, the total noise current spectrum density of the complementary type VCO in Fig. 6 can be expressed as:

$$\sum\frac{\overline{i_n^2}}{\Delta f} = \left[\frac{\overline{i_{Md,n}^2}}{\Delta f}+\frac{\overline{i_{Md,p}^2}}{\Delta f}+\frac{\overline{i_{Mg,n}^2}}{\Delta f}+\frac{\overline{i_{Mg,p}^2}}{\Delta f}\right]+\left[\frac{\overline{i_{n,tank}^2}}{\Delta f}\right] \quad (5)$$

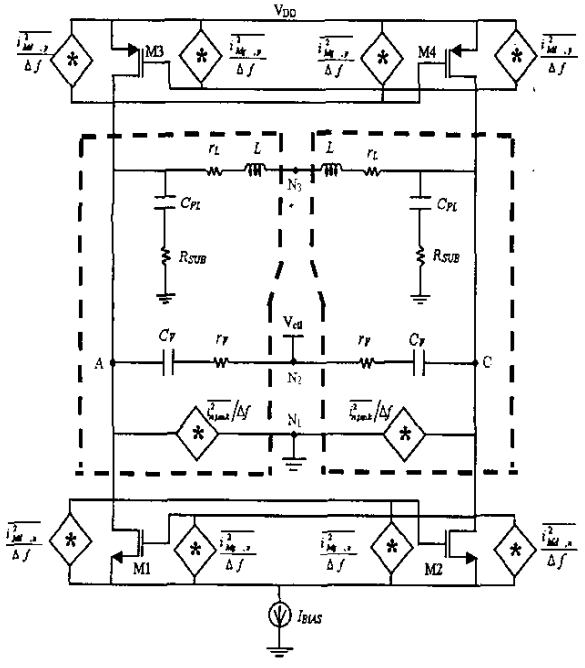


Fig. 6. A complementary type VCO with noise sources associated with the LC tank circuits and core MOSFETs. Nodes N_1, N_2, and N_3 are denoted as AC grounds.

The noise current spectrum density generated in the LC tank circuits is dictated by the layout and is independent of the sizes of the core MOSFETs. Therefore, to minimize (5) subject to the gate length of the MOSFETs is equivalent to minimizing the term inside the first bracket in (5), and the objective function can be expressed in terms of the gate length, L, as follows.

$$f(L) = \frac{\overline{i_{Md,n}^2}}{\Delta f}+\frac{\overline{i_{Md,p}^2}}{\Delta f}+\frac{\overline{i_{Mg,n}^2}}{\Delta f}+\frac{\overline{i_{Mg,p}^2}}{\Delta f} \quad (6)$$

From (2), it is clear that the first and second terms in (6) are inversely proportional to the gate length, L. In (3), the third and fourth terms in (6) appeal proportional to the gate length, L, at first glance. However, the C_{gs} term in (3) also depends on the gate length. It is necessary to express (3) in terms of the gate length exclusively, and a further simplification for the C_{gs} term is required. Since the MOSFETs in a VCO operate in both the triode and saturation regions within each period, the gate-to-source capacitance, C_{gs}, can be estimated by

$$C_{gs} \approx \frac{1}{2}\left(\frac{1}{2}+\frac{2}{3}\right)C_{ox}WL = \frac{7}{12}C_{ox}WL \quad (7)$$

where W is the gate width of the transistor. With the aspect ratio, $S=W/L$, (7) can be further simplified, and the transistor's gate noise current spectrum density in (3) can be expressed as:

$$\frac{\overline{i_{Mg}^2}}{\Delta f} = \left[\frac{49\,kT\,\delta\omega^2 S^2 C_{ox}^2 E_{sat}}{180\,I_{dc}}\right]L^5 \equiv \alpha_2 L^5 \quad (8)$$

Merging (2) and (8) into (6) results in:

$$f(L) = \frac{\alpha_1}{L}+\alpha_2 L^5 \quad (9)$$

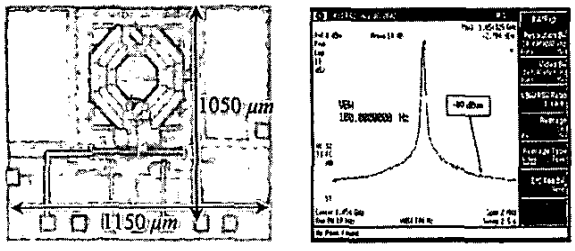
The minimum of the objective function in (9) occurs at the optimum gate length, L_{opt}:

$$L_{opt} = \sqrt[6]{\frac{\alpha_1}{5\alpha_2}} \equiv \eta\cdot L_{\min} \text{ where } \eta = \frac{1}{L_{\min}}\sqrt[6]{\frac{\alpha_1}{5\alpha_2}} \quad (10)$$

Equation (9) manifests the existence of the optimum gate length, L_{opt}, of the core MOSFETs for minimum phase noise. It also predicts a funnel shape curve for the plot of phase noise versus gate length for a fixed aspect ratio, S.

IV. The Design Of Three 1 GHz VCOs

Based on the analysis in Section III, three 1 GHz complementary type VCOs with the same LC tank circuits, but different MOSFET sizes (Fig. 6) were designed. The I_{BIAS} current is specified to be 24 mA. V_{DD} is 5 volts so that the signal level at nodes A and C is 2 V_{pp}. The passive LC tank is completely characterized in Figures 2 and 5. Two source followers are connected to nodes A and C, respectively, and were designed to drive a 50 Ω load. The objective is to determine the size of each MOSFET in Fig. 6. For symmetry of the output waveform, M1=M2 and M3=M4. The voltage drop of the constant current sink is 1 volt, and nodes A and C in Fig. 6 are biased at 3 volts. By compensating enough negative resistance to initiate the oscillation, the aspect ratios for M1 and M3 are found, and Table I summarized the MOSFET sizes of three different designs. The target center frequency was 1 GHz and the measured center frequency drifted a little due to the increased parasitic capacitance of larger sizes of the MOSFETs. In Table I, "Identifier 2" is the oscillator with optimal sizing of the MOSFETs for minimum phase noise. Fig. 7(a) shows the layout of the "Identifier 2" in Table I, and Fig. 7(b) shows the measured phase noise at 600 kHz offset from the center frequency. Fig. 8 summarizes the phase noise performance for each case, and there is a 2 dBc/Hz difference between cases 1 and 2. The funnel shape in Fig. 8 supports the prediction in (9).



(a) (b)

Fig. 7. "Identifier 2" (a) layout and (b) phase noise at 600 kHz offset measured by the HP4401B spectrum analyzer.

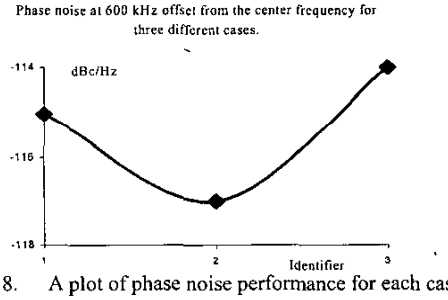


Fig. 8. A plot of phase noise performance for each case.

Table I. A summary of three different 1 GHz VCOs.

f_0 (GHz)	Identifier	M1=M2 (NMOS)	M3=M4 (PMOS)
1.250	1 (L=0.6 μm)	$S = 92\left(\frac{3.15\mu m}{0.6\mu m}\right) = 483$	$S = 172\left(\frac{3.60\mu m}{0.6\mu m}\right) = 1032$
1.060	2 (L=0.9 μm)	$S = 92\left(\frac{4.80\mu m}{0.9\mu m}\right) = 490$	$S = 172\left(\frac{5.40\mu m}{0.9\mu m}\right) = 1032$
0.926	3 (L=1.0 μm)	$S = 92\left(\frac{6.30\mu m}{1.2\mu m}\right) = 483$	$S = 172\left(\frac{7.20\mu m}{1.2\mu m}\right) = 1032$

V. Conclusions

The noise sources associated with the passive LC tank circuits and core MOSFETs are analyzed. Based on this analysis, there exists an optimum gate length to minimize the phase noise without introducing severe frequency shift. Three 1 GHz VCOs with the same LC tank circuits, but different MOSFET sizes were designed, fabricated, and tested. The measured phase noise performance supports the theoretical predictions.

Acknowledgement

The authors wish to acknowledge the assistance and support of Texas Instruments and the sponsoring member companies of the Georgia Tech Analog Consortium.

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